Vertical and Lateral Copper Transport through Graphene Layers

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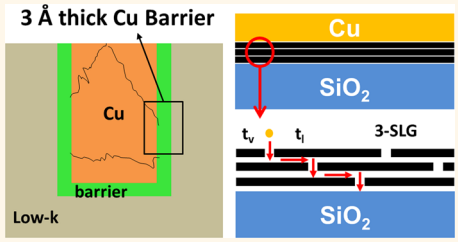
ABSTRACT A different mechanism was found for Cu transport through multi-transferred single-layer graphene serving as diffusion barriers on the basis of time-dependent dielectric breakdown tests. Vertical and lateral transport of Cu dominates at different stress electric field regimes. The classic E-model was modified to project quantitatively the effectiveness of the graphene Cu diffusion barrier at low electric field based on high-field accelerated stress data. The results are compared to industry-standard Cu diffusion barrier material TaN. 3.5 Å single-layer graphene shows the mean time-to-fail comparable to 4 nm TaN, while two-time and three-time transferred single-layer graphene stacks give 2× and 3× improvements, respectively, compared to single-layer graphene at a 0.5 MV/cm electric field. The influences of graphene grain boundaries on Cu vertical transport through the graphene layers are explored, revealing that large-grain (10−15 μm) single-layer graphene gives a 2 orders of magnitude longer lifetime than small-grain (2−3 μm) graphene. As a result, it is more effective to further enhance graphene barrier reliability by improving single-layer graphene quality through increasing grain sizes or using single-crystalline graphene than just by increasing thickness through multi-transfer. These results may also be applied for graphene as barriers for other metals.



KEYWORDS: graphene · interconnect · Cu diffusion barrier · time-dependent dielectric breakdown (TDDB) · modified E-model · back-end-of-the-line (BEOL) · reliability

Along the way to advance Moore's Law, the escalation of the interconnect RC delay has diminished the gains made from transistor scaling. Indeed, beyond the 16 nm technology node, the global/intermediate interconnect RC delay is over 1000 times longer than transistor delay.[1] The transistor scaling still continues, yet there are not many ways to improve the performance of interconnects, and moving forward to smaller wire pitches, the interconnect resistance is projected to rise rapidly.[2] The use of Cu as wires requires a diffusion barrier layer (Figure 1a) to prevent Cu from diffusing into the dielectric and the silicon and cause dielectric breakdown and create deep level traps in silicon. The resistivity of the industrial standard TaN barrier is around 260−290 $\mu\Omega\cdot$cm, much higher than that of bulk Cu (~1.67 $\mu\Omega\cdot$cm). To achieve small overall interconnect resistivity, more conductive and thinner barrier materials are needed. Many advanced barrier materials are being explored: Ru/Ti has low resistance and reasonable barrier reliability,[3] MnO_x gives thin thickness and good reliability[4,5] but has very high resistivity, and CoW alloy shows low resistivity and good adhesion to Cu.[6] However, these materials all face problems scaling down to atomic thickness.

According to the ITRS,[2] the barrier will need to thin down to 3 Å. So far, only single layer graphene can meet this requirement. Aside from being atomically thin, graphene is impermeable as a gas membrane including helium and effective in protecting Cu or Cu/Ni alloys from oxidation.[7,8] Thus, it is expected that graphene may also be impermeable to Cu atoms. Graphene also has high conductivity (1−100 $\mu\Omega\cdot$cm),[9,10] which helps retain Cu interconnect effective resistivity even when wire pitches scale down to 10 nm.[11] Moreover, wrapping graphene around the Cu nanowire structure protects Cu from oxidizing and thus minimizes surface scattering, leading to a resistivity even lower than that of the bare Cu interconnect.[12] Graphene/copper composites have the advantages of being able to conduct higher current density and sustain higher breakdown voltage compared to bare Cu wires.[13] Furthermore, the superior thermal conductivity of graphene[14] enhances the graphene/Cu thermal reliability.[12]

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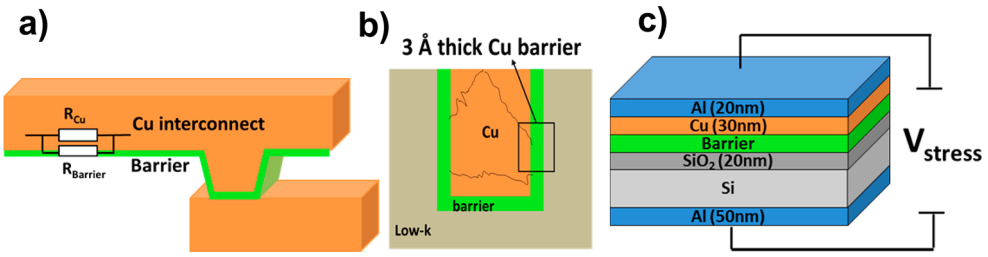

Figure 1. (a) Schematic of the interconnect with diffusion barrier, (b) cross-section of the interconnect with 3.5 Å SLG barrier, (c) planar capacitor TDDB test structure for evaluating different Cu diffusion barriers.

Thus, graphene is a leading candidate to replace TaN as the next-generation Cu diffusion barrier.

Previously, it has been shown that the as-grown trilayer graphene is thermally stable against Cu diffusion up to 750 °C.[15] The effectiveness of graphene as a diffusion barrier has been studied from a material characterization standpoint by X-ray diffraction, transmission electron microscopy, and time-of-flight secondary ion mass spectroscopy analyses.[16] A model for Cu transport in graphene barriers has been presented,[17] and the penetration and lateral diffusion of environmental molecules in polycrystalline graphene have been characterized.[18] Nevertheless, most of these works only focused on material characterizations. In a recent report, the reliability of graphene as a Cu diffusion barrier has been proven through electrical measurements and benchmarked to industry standard material TaN.[11] The Cu transport process must be elucidated to enable graphene reliability assessment and accelerate the use of graphene as barrier for Cu and other metals in industry.

Here, we present a quantitative analysis of the Cu transport process using electrical measurements of the time-dependent dielectric breakdown (TDDB) test. The metric we use is the mean time-to-fail (MTTF) from the TDDB test, and we compared the performance of graphene with TaN of various thicknesses at high electric field stress. The MTTF of the structure with a multi-transferred single-layer graphene (SLG) barrier cannot be described by the classic E-model.[19] To explain the experimental observation, a new Cu ion-transport process is revealed and a modified E-model is developed. The vertical and lateral transport processes of Cu ions are further analyzed by temperature dependent test. The influences of graphene grain boundaries for vertical transport are studied, leading to approaches for further SLG reliability improvement.

RESULTS AND DISCUSSION

A simplified MOS capacitor structure (Figure 1 c) is used to test the reliability of different barriers.[20] Using this structure, MTTF of the structure with graphene and TaN barriers of various thicknesses under TDDB testing is examined. To evaluate the reliability and Cu blocking capability of graphene, the following graphene stacks are compared against 2 and 4 nm TaN: SLG, bilayer

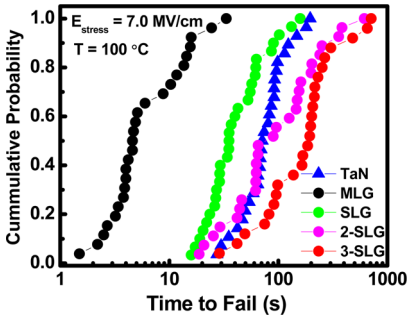

Figure 2. Statistical distribution of the TDDB lifetime with SLG, 2-SLG, 3-SLG, MLG, and 4 nm TaN at 7.0 MV/cm electric field and 100 °C temperature stress.

graphene (2-SLG) obtained by transferring SLG two times, trilayer graphene (3-SLG) obtained by transferring SLG three times, and 4 nm multilayer graphene (MLG) grown by CVD on Ni. The quality of the transferred graphene was checked by Raman spectroscopy (Figure S1).[21] The D peak to G peak intensity ratio $I_D/I_G \sim 0.2$ of MLG indicates worse quality in comparison with SLG, 2-SLG, and 3-SLG. The thickness of the SLG, 2-SLG, and 3-SLG are 0.35, 0.71, and 1.41 nm from AFM. The thicknesses of 2-SLG and 3-SLG are slightly larger than the exfoliated two-layer (0.69 nm) and three-layer graphene (1.125 nm) due to the transfer process.[22] The thickness of MLG and TaN are confirmed to be 4 nm by transmission electron microscopy (TEM) (Figure S2).

Figure 2 indicates that compared to the 4 nm TaN barrier, the 4 nm MLG and 0.35 nm SLG barrier fails more quickly, but the 0.71 nm 2-SLG has a longer time to fail and 3-SLG gives a ~2× longer lifetime. The MTTF of the structure with stacked SLG, MLG, and TaN barriers are summarized in Figure 3. The structure's MTTFs with SLG, 2-SLG, and 3-SLG barrier are 48.9 s, 140 and 214 s, respectively. These correspond to the MTTF of 4 nm TaN (82.4 s) being 0.6×, 1.7×, and 2.6× longer, while the MTTF of MLG (12.5 s) is only about 0.15× because of the higher defect density (Figure S1) at the 7.0 MV/cm electric field and 100 °C temperature stressing condition. On the other hand, the MTTF of the structure drops by 5.6× when the TaN thickness scaled from 4 to 2 nm. On this basis, more MTTF degradation is expected when the TaN thickness shrinks further to the atomic scale, at which point SLG would give a superior

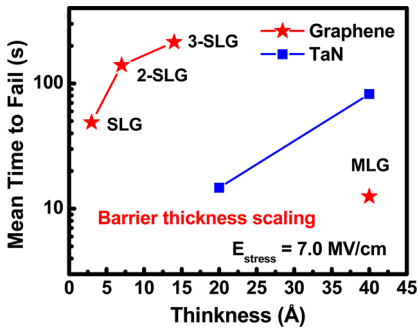

Figure 3. Structure's MTTF with barrier thickness scaling stressed at a 7.0 MV/cm electric field and 100 °C temperature stressing condition.

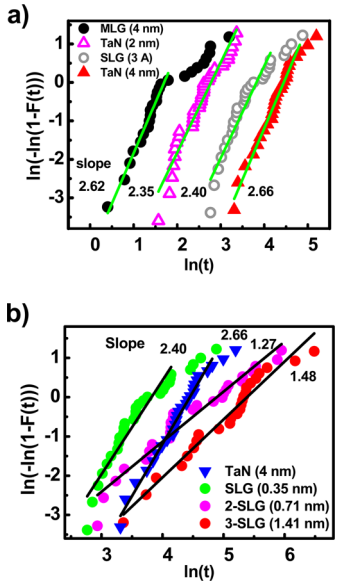

Figure 4. Weibull distribution of the TDDB lifetime of the structures (a) with MLG, TaN and SLG barriers and (b) with SLG, 2-SLG, 3-SLG, and TaN barriers.

MTTF. Meanwhile, the MLG shows worse MTTF than SLG due to the higher density of disorders in MLG as shown in the Raman spectrum (Figure S1).[11,23]

Larger distribution variations have been observed with 2-SLG and 3-SLG than with SLG and TaN. The Weibull distribution eq 1[24]is used to quantify this:

$$\ln[-\ln(1-F(t))] = \beta \ln(t) - \ln(\alpha) \qquad (1)$$

Here, $F(t)$ is the statistical distribution of the lifetime, t is the MTTF, α is the scale parameter, and β is the shape parameter or Weibull slope. As shown in Figure 4, the values of the Weibull slope β with SLG, MLG, or TaN are almost the same at ~2.5, while those with 2-SLG and 3-SLG are almost two times smaller at ~1.4. This indicates that there may be a different Cu ion-transport process for stacked graphene layers since Cu ions are the main reason for dielectric breakdown below the critical electric field (Figures S3 and S4).

For the 3-SLG barrier (Figure 5), Cu ions need to penetrate both vertically and laterally from one layer to

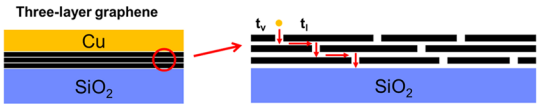

Figure 5. Schematic of the Cu ion-transport process through 3-SLG.

another since the defects in every layer are independent. The vertical transport time is proportional to the vertical electric field, as the E-model[19] used for MTTF prediction can be applied here in the form $t_v \sim \exp(-\gamma E_{stress})$; on the other hand, the lateral transport time is independent of the vertical electric field and is proportional to the diffusion coefficient D and activation energy E_b: $t_l \sim D\exp(E_b/(kT))$. The total time t_{tot} through the SLG stacks is the sum of these two components: $t_{tot} = t_v + t_l$.

However, the E-model in eq 2 cannot fit the 2-SLG and 3-SLG barrier experimental data.

$$\text{MTTF} \sim \text{A}\cdot\exp\left(\frac{E_a}{k_B T} - \gamma E_{stress}\right) \qquad (2)$$

The 1/E-model[25] and $\sqrt{E}$-model[26,27] also do not fit the data as these models all give a smaller slope parameter γ and thus a smaller MTTF than that with TaN barriers at low electric field despite the fact that multistacked SLG showed longer MTTF at high electric fields. Taking into account the new Cu ion-transport process discussed above, the modified E-model for multistacked SLG is

$$\text{MTTF} \sim D\exp\left(\frac{E_b}{k_B T}\right) + A\exp\left(\frac{E_a}{k_B T} - \gamma E_{stress}\right) \qquad (3)$$

For simplicity, we can assume that the electric field stress factor γ is the same for both the graphene layer and the dielectric layer with sufficient accuracy. The E-model is chosen here because different dielectric lifetime prediction models result in different lifetimes at low electric fields but still give the same trend for different barrier materials. Among these models, the E-model gives the most conservative prediction at low electric fields.[28] Note that here we focused on developing a model for MTTF quantitative prediction at low electric fields but not on the physical transport process of Cu species at the atomic scale.

With the modified E-model, the vertical transport t_v is much larger than lateral transport t_l and dominates at extremely low electric field regime. With negligible t_l, the MTTF of multi-transferred graphene stacks vs electric field curve should be close to that of the SLG barrier. On the other hand, at high electric fields, t_l is much larger than t_v and dominates. Since t_l is independent of the vertical electric fields, it should be constant regardless of the electric field change. Ideally, at high enough electric fields, if t_{tot} is not affected by the intrinsic breakdown, then only t_l would be left and its value could be extracted. However, beyond the critical electric field (Figure S4), intrinsic breakdown

dominates. In other words, the breakdown would not be due to the diffusion of Cu ions and t_l would not matter. As a result, t_l cannot be extracted in practical situations.

Alternatively, at high electric field that remains below the critical electric field, t_l is closer to the experimentally extracted MTTF. To make a practical prediction, we use the MTTF with SLG barrier at 8.5 MV/cm (lower than the critical breakdown voltage). For a first-order estimation, t_v with 2-SLG and 3-SLG are assumed to be two and three times of that with SLG barrier, respectively; $t_{v(2-SLG)} = 2t_{v(SLG)}$, $t_{v(3-SLG)} = 3t_{v(SLG)}$. Next, t_l can be extracted by subtracting t_v from the $MTTF_{E=8.5\ MV/cm}$ or $t_l = MTTF_{E=8.5\ MV/cm} - t_v$. Since t_l is the same under different electric fields, $t_v(E)$ at different electric fields are obtained by subtracting t_l from MTTFs at different electric fields: $t_v(E) = MTTF(E) - t_l$. We can then linearly fit the $t_v(E)$ vs E curve and use the slope and intercept to arrive at a new value of t_v' at 8.5 MV/cm, which is used to calibrate the previous first order estimation. After iterating two or three times, the calibrated lateral transport time t_l with 2-SLG and 3-SLG were 16.6s and 27.9s, respectively. The latter value is almost twice of the former one since Cu ions travel laterally twice in 3-SLG and only once in 2-SLG and the time to travel laterally between every layer is roughly the same. The values of the slope parameter γ with one- to three-layer graphene barriers are 1.31, 1.28, and 1.29, respectively. In theory, the thicker the graphene layers are, the larger the slope parameter γ should be. The small deviation from the theory of similar slope parameter for various graphene layers is due to inevitable experimental error, as well as fitting errors.

The low-field prediction presented in Figure 6 is based on the modified E-model and calibrated data. The MTTF improvement for 2-SLG and 3-SLG at low fields are not as large as at high fields, showing only two and three times longer lifetime than SLG, respectively. This is because the extra lateral ion transport time is negligible at low fields. In other words, the advantage of multistacked SLG over SLG is not as high as we would expect if we only focus on high electric field data and assume a conventional model that does not involve lateral Cu transport between graphene layers. The lateral transport is not important in MLG because of the high defect density and large defect sites.

A temperature-dependent analysis of the MTTF of graphene with various thicknesses was conducted as well. As shown in Figure 7a, the MTTF decreases with higher temperature and increases with thicker graphene as expected. In Figure 7b, the MTTFs with respect to temperature are shown, which are typically used to extract the activation energy E_a of the E-model. Following this method, E_a for the structure without any barriers and with a SLG barrier were extracted to be 0.69 and 0.66 eV, respectively.

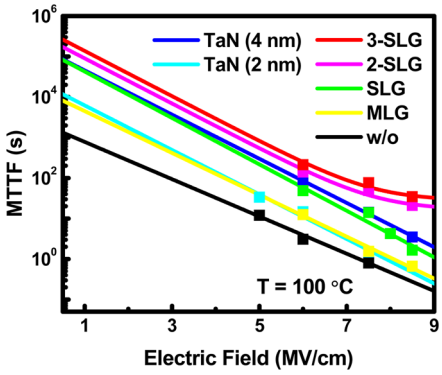

Figure 6. MTTF vs electric field at 100 °C with different barrier materials based on the E-model and modified E-model.

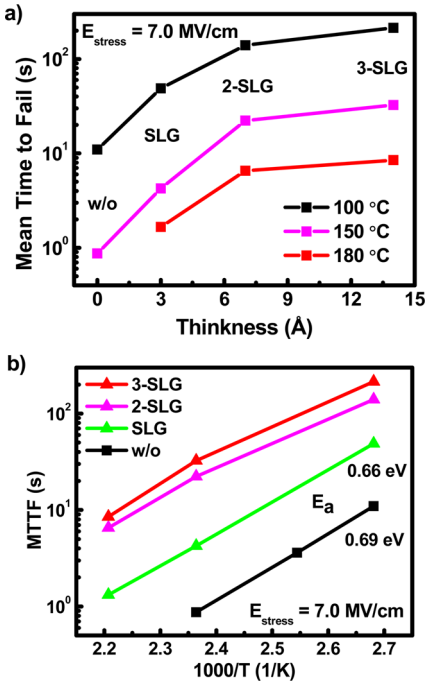

Figure 7. MTTF of structures: (a) with barrier thickness scaling under different temperature stressing; (b) with temperature scaling for graphene with varying thicknesses.

The insertion of a barrier layer between Cu and the dielectric makes the interpretation of the activation energy a bit complicated. For the E-model, dielectric breakdown was proposed to occur when a conductive percolation path is formed in the oxide when enough defects form within the oxide.[29,30] At higher stressing temperatures, Cu ions or atoms carry higher energy, leading to easier formation of the conductive path. Therefore, the activation energy, or the energy to break the Si—O or Si—Si bond of the oxide,[29,31] extracted here is almost the same for the structures with or without barriers because defect formation is the dominant temperature-dependent process. On the other hand, with the multistacked graphene barrier, the log(MTTF) curve shows a nonlinear relation with $1/T$, which very likely results from the influence of the lateral transport as shown in the modified E-model (eq 3)

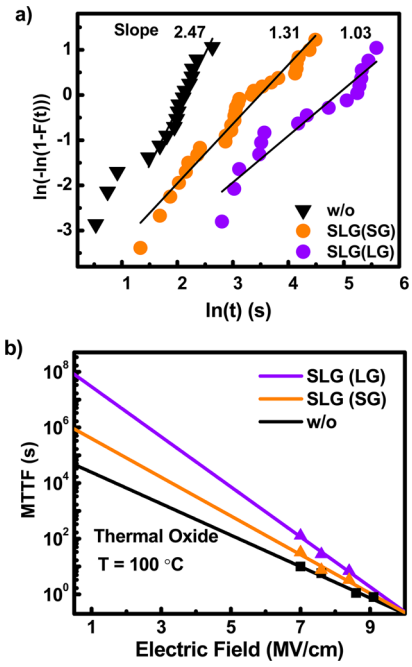

Figure 8. (a) Weibull distribution of the TDDB lifetime of the structure with SLG of different grain sizes (LG: large grain of 10−15 μm; SG: small grain of 2−3 μm); (b) MTTF vs electric field at 100 °C with SLG of different grain sizes based on the E-model.

besides the experimental uncertainty. The activation energy E_a therefore cannot be extracted from these two sets of data.

Previous work has shown that better TDDB performance can be achieved with cleaner graphene-transfer methods and large-grain graphene.[11] Here, we explore further how the defects in SLG influence the graphene reliability and Cu vertical transport quantitatively. Denser dry thermal SiO_2 (instead of CVD SiO_2) is used here to focus on the barrier intrinsic performance by reducing the influence of transfer-induced defects. SLG shows longer MTTF than 4 nm sputtered TaN as can be seen in Figure S5.

SLGs with varying grain sizes were used for the thermal oxide TDDB test to reveal the influence of grain boundaries. Detailed information about SLG grain size is in ref 32. As shown in Figure 8a), it takes ~4× longer time to fail with SLG of large grain (10−15 μm) than that of small grain (2−3 μm).[32] Even so, for large-grain SLGs under test devices of the same area, some devices may have more grain boundaries than others, causing larger variation in lifetime. On the other hand, for a given area, the numbers of grain boundaries for small-grain SLGs are almost the same, giving less variation.

Figure 8b shows the low electric field projection from the E-model for SLG of different grain sizes. The large-grain SLG gives a larger slope parameter γ of 2.1 than the small-grain SLG of 1.6. As a result, when SLG grain size increases from 2 to 3 μm to 10−15 μm, there is 2 orders of magnitude improvement for the MTTF at electric field of 0.5 MV/cm. Based on this trend, orders of magnitude MTTF enhancement is expected when using graphene with even larger-grain size or ultimately single-crystalline graphene as is now viable.[33] Furthermore, compared to the MTTF with the multi-transferred SLG stacks barrier in Figure 6, more reliability enhancement can be achieved from SLG graphene quality improvement. At this point the quality of graphene is more important than the number of graphene layers or thickness. Besides the grain boundaries, some other defects in graphene like pinhole defects, transfer-induced defects may also influence the performances.

There are still several problems to be solved before graphene can be introduced as Cu diffusion barrier in industry. The first one is how to integrate graphene to traditional Cu electroplating process and damascene process.[34] One possible solution is to develop an approach to grow graphene around Cu interconnect after Cu electroplating. Another problem is the poor adhesion of transferred graphene to both the dielectric and Cu. However, since Cu is used as catalyst for single-layer graphene CVD synthesis, the as-grown graphene has no adhesion problem with the Cu catalyst.

CONCLUSIONS

In conclusion, through TDDB test, the scaling potential of multi-transferred 1−3 layer (0.35−1.41 nm) graphene is demonstrated to be better than industrial standard material TaN (2−4 nm) as a Cu diffusion barrier. In addition, both lateral and vertical Cu ion transport processes are found in stacked graphene barriers, although they dominate in different electric field regimes. A modified E-model is proposed to project the MTTF of the structure with stacked graphene revealing its limited advantage over single layer graphene. On the other hand, large-grain (10−15 μm) SLG gives 2 orders of magnitude improvement over small-grain (2−3 μm) SLG at low electric fields, indicating large room for further improvement with larger-grain SLG or even single-crystalline graphene.

METHODS

The structure starts with 20 nm SiO_2 grown on a silicon wafer. Two different kinds of silicon oxides are used, CVD oxide and thermal oxide grown at 900 °C in dry O_2 ambient. Graphene is then transferred onto the surface of the oxide using a modified RCA clean method.[35] SLG is CVD grown on Cu foil and MLG is CVD grown on Ni foil purchased from Graphene Supermarket.[36] Next, the graphene is patterned to 100 μm × 100 μm square pads using oxygen plasma. After that, Cu and Al are evaporated as the top gate electrode. Then, the backside SiO_2 is removed using 50:1 hydrogen chloride (HF) and Al is deposited as a back

electrode. Finally, the sample is annealed in forming gas for 30 min at 300 °C. Using the same process flow, the same structures with a PVD TaN barrier and without any barrier (for comparison) were fabricated.

The various grain sizes of single-layer graphene are obtained by adjusting the temperature and the carbon concentration during the CVD growth process. Prior to the growth, the Cu foils were annealed in a reducing forming gas environment (17 sccm H_2, 320 sccm Ar) at their respective growth temperatures for 30 min to remove any surface oxides. Graphene of 3 μm grains was grown in a 0.360 sccm CH_4, 17 sccm H_2, and 320 sccm of Ar flow at 972 °C for 240 min, while graphene of 14 μm grains was nucleated in a 0.250 sccm CH_4, 17 sccm H_2, and 320 sccm of Ar flow at 1030 °C conditions for 240 min. The average grain sizes were calculated by measuring the spatially averaged internucleation distance from the SEM images of partial grown graphene under the same conditions.[32]

Raman spectra were acquired using a WiTec 500 AFM/micro-Raman Scanning microscope, equipped with a 532 nm wavelength laser and a 600 lines/mm grating.

The TEM samples were prepared using the in situ FIB lift out technique on an FEI Strata Dual Beam FIB/SEM. The target areas were covered with carbon ink and an iridium protective layer, followed by e-beam and i-beam deposited Pt as an overcoat during FIB milling. The samples were imaged with a JEOL TEM operated at 200 kV in bright-field (BF) mode and high-resolution (HR) mode.[37]

Conflict of Interest: The authors declare no competing financial interest.

Supporting Information Available: The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.5b03038.

Raman spectrum of MLG, SLG, 2-SLG, and 3-SLG, TEM image of MLG and TaN, and breakdown voltage and breakdown mechanism (Figures S1−S6) (PDF)

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